

CLAIMS

1 1. A lateral thyristor structure for protection against electrostatic discharge, comprising:
2 a semiconductor substrate (20) of a first conduction type, with a surface;
3 a well region (21) of a second conduction type, opposite to said first conduction type,
4 which is introduced into said surface of said semiconductor substrate;
5 a first strongly doped region (22) of said second conduction type that is introduced into
6 said surface of said semiconductor substrate (20) and is electrically connected to a first
7 terminal (26);
8 a second strongly doped region (23) of said first conduction type that is introduced into
9 said well region (21) and is electrically connected to a second terminal (27);
10 a third strongly doped region (24) of said second conduction type, which is introduced
11 into said well region (21), is electrically connected to said second terminal (27), and is
12 spatially arranged between said first strongly doped region (22) and said second strongly doped
13 region (23); and
14 a fourth strongly doped region (25) of said second conduction type, which is introduced
15 into said surface of said semiconductor substrate (20) and into said well region (21), and is
16 spatially situated above a pn junction that is formed between said semiconductor substrate (20)
17 and said well region (21), and between said third strongly doped region (24) and said first
18 strongly doped region (22).

A1 2. The lateral thyristor structure of claim 1, comprising a field oxide region (28) that is situated between said first strongly doped region (22) and said fourth strongly doped region (25).

1 3. The lateral thyristor structure of claim 1, comprising a field oxide region (29) that is
2 situated between said second strongly doped region (23) and said fourth strongly doped region
3 (25).

B2 1 4. The lateral thyristor structure of claim 3, wherein said first conduction type is p-
2 conducting and said second conduction type is n-conducting.

1 5. The lateral thyristor structure of claim 4, wherein said first terminal is connected to
2 ground, and said second terminal is connected to a signal input line or to a signal output line.

SUB3 1 6. The lateral thyristor structure of claim 5, comprising a region (41) of said second
2 conduction type, and including a terminal (40) that is introduced into a field oxide region (29,
3 30), wherein said terminal (40) is connected to a circuit (4) that is being protected.

1 7. The lateral thyristor structure of claim 6, wherein said thyristor structures comprise at
2 least two component structures.

SUB3 1 8. The lateral thyristor structure of claim 7, wherein said component structures are
2 surrounded by a substrate contact ring (31).

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1 9. The lateral thyristor structure of claim 7, wherein said component structures are
2 arranged symmetrically, and in such that said active regions adjoin one another closely, while
3 said substrate contacting ring is removed as far as possible from said active region.

1 10. The lateral thyristor structure of claim 7, wherein said active regions adjoin one
2 another closely, while said substrate contact ring is removed as far as possible from said active
3 region.

1 11. The lateral thyristor structure of claim 7, wherein said component structures are
2 arranged symmetrically, and in such that said active regions adjoin one another closely, while
3 said substrate contacting ring is removed from said active region.

1 12. A lateral thyristor structure for protection against electrostatic discharge, comprising:
2 a semiconductor substrate of a first conduction type, with a surface;
3 a well region of a second conduction type, opposite to said first conduction type, which
4 is introduced into said surface of said semiconductor substrate;
5 a first strongly doped region of said second conduction type that is introduced into said
6 surface of said semiconductor substrate and is electrically connected to a first terminal;
7 a second strongly doped region of said second conduction type that is introduced into
8 said well region and is electrically connected to a second terminal;
9 a third strongly doped region of said second conduction type, which is introduced into
10 said well region, is electrically connected to said second terminal, and is spatially arranged
11 between said first strongly doped region and said second strongly doped region; and

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12 a fourth strongly doped region of said second conduction type, which is introduced into
13 said surface of said semiconductor substrate and into said well region, and is spatially situated
14 above a pn junction that is formed between said semiconductor substrate and said well region,
15 and between said third strongly doped region and said first strongly doped region.

புது திட்டங்கள் மூலம் நாம் நாட்டை விரிவாக்க வேண்டும்.